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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/676,771 | 10/01/2003 | Tsung-Hsin Yu | 67,200-1115 | 7894 |

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| EXAMINER | |
|---|---|
| COX, CASSANDRA F | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/676,771 | YU, TSUNG-HSIN | |
| | Examiner | Art Unit | |
| | Cassandra Cox | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-22* is/are rejected.

7)☒ Claim(s) *23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's arguments filed 05/19/06 have been fully considered but they are not persuasive. The rejection is repeated below.

## EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Randy Tung on December 06, 2005.

The application has been amended as follows: In line 20 of claim 19 the word "second" has been replaced by the word --first--.

In line 21 of claim 19 the word "first" has been replaced by the word --second--.

In line 7 of claim 20 the word "second" has been replaced by the word --first--.

In line 9 of claim 20 the word "first" has been replaced by the word --second--.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 19-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (U.S. Patent No. 6,492,848)

5. In reference to claim 19 Lee discloses in Figure 2 a power-on bias circuit comprising: a first inverter (PM21, NM21) having an input terminal (N20) and an output terminal (N21), the input terminal of the first inverter functions as a first voltage input terminal for the power-on bias circuit; a second inverter (INV21) having an input terminal and an output terminal, wherein the output terminal of the second inverter functions as an output terminal for the power-on bias circuit; and a Schmitt Trigger circuit (231) comprising: a first P-type transistor (PM13), a second P-type transistor (PM14), wherein a substrate of the second P-type transistor (PM14), a substrate and a source region of the first P-type transistor (PM13) are electrically connected to a second voltage input terminal (P_ON) of the power-on bias circuit (while the circuit does not specifically shown the connection of the substrates to the second voltage input terminal, it is considered to be well-known to one skilled in the art that the substrate of a p-type transistor will typically be tied to the higher voltage potential, of which fact official notice is taken), a source region of the second P-type transistor (PM14) is electrically connected to a drain region of said first P-type transistor (PM13); a first N-type transistor (NM13); a second N-type transistor (NM14), a gate of the first P-type transistor (PM13), a gate of the second P-type transistor (PM14), a gate of the first N-type transistor (NM13) and a gate of the second N-type transistor (NM14) are electrically connected to the input terminal for the Schmitt Trigger circuit (231), the input terminal of the Schmitt

Trigger circuit is electrically connected to the output terminal of the first inverter (PM21, NM21), a substrate of the first N- type transistor (NM13), a substrate and a source region of the second N-type transistor (NM14) are electrically connected to ground (while the circuit does not specifically shown the connection of the substrates to the second voltage input terminal, it is considered to be well-known to one skilled in the art that the substrate of a n-type transistor will typically be tied to the lower voltage potential, of which fact official notice is taken), a drain region of the second N-type transistor (NM14) is electrically connected to a source region of the first N-type transistor; a third P-type transistor (PM15), a source region of the third P-type transistor (PM15) is electrically connected to the drain region of the first P-type transistor (PM13) and the source region of the second P-type transistor (PM14), a drain region of the third P-type transistor (PM15) is electrically connected to ground, a substrate of the third P-type transistor is electrically connected to the second voltage input terminal (P_ON) (while the circuit does not specifically shown the connection of the substrates to the second voltage input terminal, it is considered to be well-known to one skilled in the art that the substrate of a p-type transistor will typically be tied to the higher voltage potential, of which fact official notice is taken) of the power-on bias circuit; and a third N-type transistor (NM15), a source region of the third N-type transistor (NM15) is electrically connected to a source region of the first N-type transistor (NM13) and a drain region of the second N-type transistor (NM14), a drain region of the third N-type transistor is electrically connected to the second voltage input terminal (P_ON) of the power-on bias circuit, a substrate of the third N-type transistor (NM15) is electrically

connected to ground (while the circuit does not specifically shown the connection of the substrates to the second voltage input terminal, it is considered to be well-known to one skilled in the art that the substrate of a n-type transistor will typically be tied to the lower voltage potential, of which fact official notice is taken), a drain region of the second P-type transistor (PM14), a drain region of the first N-type transistor (NM13), a gate of the third P-type transistor (PM15) and a gate of the third N-type transistor (NM15) are electrically connected to the output terminal of the Schmitt Trigger circuit, the output terminal of the Schmitt Trigger circuit is electrically connected to the input terminal of the second inverter (INV21).

6. In reference to claim 20 Lee also discloses in Figure 2 that the first inverter (PM21, NM21) comprises a fourth P-type transistor (PM21) and a fourth N-type transistor (NM21), a substrate and a source region of said fourth P-type transistor is electrically connected to the second voltage input terminal (P_ON) (while the circuit does not specifically shown the connection of the substrates to the second voltage input terminal, it is considered to be well-known to one skilled in the art that the substrate of a p-type transistor will typically be tied to the higher voltage potential, of which fact official notice is taken) of the power-on bias circuit, a source region of said fourth N-type transistor (NM21) is electrically connected to ground, a gate of the fourth P-type transistor (PM21) and a gate of the fourth N-type transistor (NM21) are electrically connected to the input terminal (N20) of the first inverter, a drain region of the fourth P-type transistor (PM21) and a drain region of the fourth N-type transistor (NM21) are electrically connected to the output terminal of the first inverter. The same applies to

claim 21, wherein it is considered obvious to one skilled in the art that the second inverter may include a fourth P-type and a fourth N-type transistor having the recited connections, since inverters in transistor layout are well known in the art.

7. In reference to claim 22 Lee discloses in Figure 2 that the first voltage input terminal (N20) of the power-on-bias circuit is a core voltage input terminal, and the second voltage input terminal (P_ON) of the power-on-bias circuit is an input terminal of an input/out terminal.

***Allowable Subject Matter***

8. Claims 23-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: Claim 23 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the dimension of the fourth N-type transistor is larger than the dimension of the fourth P-type transistor to reduce a leakage current flowing from the second voltage input terminal to the ground in combination with the rest of the limitations of the base claims and any intervening claims. Claim 24 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the second voltage input terminal receives a voltage signal of high potential when peripheral circuits are turned on before turning on core circuits in combination with the rest of the limitations of the base claims and any intervening claims.

### *Response to Arguments*

10. Applicant's arguments filed 05/19/06 have been fully considered but they are not persuasive. In response to applicant's argument that the node N20 of Lee is not a "first input terminal for said power-on circuit", this argument is not persuasive. The fact that this node receives a feedback voltage as input does not prohibit it from being an input terminal. Furthermore, there is nothing in applicant's claim that requires the input signal to be an external signal. The rejection is maintained.

### *Conclusion*

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

August 5, 2006

QUAN TRA
PRIMARY EXAMINER